AMENDMENTS TO THE CLAIMS

1. (Original) A method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines, comprising the steps of:

the first semiconductor device supplying a selected one of the bus lines with a first logical output signal;

the second semiconductor device acquiring a first bus line signal from the selected bus line;

the second semiconductor device inverting the first bus line signal to generate a second logical output signal;

the second semiconductor device transmitting the second logical output signal to the first semiconductor device;

the first semiconductor device receiving a second bus line signal from the selected bus line; and

the first semiconductor device comparing the first logical output signal and the second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

2. (Original) The method of claim 1, wherein the first semiconductor device supplies the selected bus line with the first logical output signal having a first logical value, and supplies the other bus lines with signals each having a second logical value.

3. (Original) The method of claim 1, wherein the first semiconductor device supplies a first bus line adjacent to a second bus line with the first logical output signal

having a first logical value, and supplies the second bus line with a signal having a second logical value.

4. (Original) The method of claim 1, wherein the first semiconductor device supplies a first group of the bus lines adjacent to a second group of bus lines with the first logical output signals each having a first logical value, and supplies the second group of the bus lines with signals each having a second logical value.

5. (Original) The method of claim 1, wherein the steps of supplying the first logical output signal, acquiring the first bus line signal, and generating the second logical output signal are executed using the selected bus line.

6. (Original) A method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines, comprising the steps of:

the first semiconductor device supplying a selected one of the bus lines with a first logical output signal;

the second semiconductor device acquiring a first bus line signal from the selected bus line;

after outputting the first logical output signal, the first semiconductor device generating a second logical output signal being an inverted signal of the first logical output signal and supplying the selected bus line with the second logical output signal;

the second semiconductor device outputting the acquired first bus line signal;

the first semiconductor device receiving a second bus line signal from the selected bus line; and

the first semiconductor device comparing the first logical output signal and the received second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

7. (Original) The method of claim 6, wherein the first semiconductor device supplies the selected bus line with the first logical output signal having a first logical value, and supplies the other bus lines with signals each having a second logical value.

8. (Original) The method of claim 6, wherein the first semiconductor device supplies a first bus line adjacent to a second bus line with the first logical output signal having a first logical value, and supplies the second bus line with a signal having a second logical value.

9. (Original) The method of claim 6, wherein the first semiconductor device supplies a first group of the bus lines adjacent to a second group of the bus lines with the first logical output signals each having a first logical value, and supplies the second group of the bus lines with signals each having a second logical value.

10. (Original) The method of claim 6, wherein the steps of supplying the first logical output signal, acquiring the first bus line signal, generating the second logical output signal, and outputting the acquired first bus line signal are executed using the selected bus line.

11. (Previously Presented) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

a first output circuit connected to one of the plurality of bus lines for supplying the bus line with a first logical output signal; and

a comparison circuit connected to the bus line; and

the second semiconductor device includes:

an input circuit connected to the bus line for acquiring a first bus line signal; and

a second output circuit connected to the input circuit for inverting the first bus line signal to generate a second logical output signal, and supplying a corresponding bus line with the second logical output signal, wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

12. (Previously Presented) The electronic device of claim 11, wherein the semiconductor device includes a plurality of first output circuits and one of the bus lines is a selected bus line, and the first output circuit corresponding to the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to the other bus lines supplies the other bus lines with signals having a second logical value.

13. (Previously Presented) The electronic device of claim 11, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line is adjacent to another bus line, and a first output circuit corresponding to the at least one bus line supplies the first bus line with the first logical output signal having a first logical value, and a first output circuit corresponding to the another bus line supplies the another bus line with a signal having a second logical value.

14. (Previously Presented) The electronic device of claim 11, wherein the first output circuit is one of a first group of first output circuits corresponding to a first group of the bus lines adjacent to a second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group of the first output circuits supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group of the first output circuits supplies the second group of the bus lines with signals each having a second logical value.

15. (Original) The electronic device of claim 11, wherein the first output circuit is used in a test mode and a normal operation mode of the first semiconductor device.

16. (Original) The electronic device of claim 11, wherein the input circuit and the second output circuit are used in a test mode and a normal operation mode of the second semiconductor device.

17. (Previously Presented) The electronic device of claim 11, wherein the input circuit includes:

a latch circuit that latches the first logical output signal, and

a reset circuit connected to the latch circuit, that resets the latch circuit in response to the first logical output signal and a command signal.

18. (Previously Presented) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

a first output circuit connected to one of the plurality of bus lines for supplying the bus line with a first logical output signal and, thereafter, supplying the bus

line with a second logical output signal being an inverted signal of the first logical output signal; and

a comparison circuit connected to the bus line; and

the second semiconductor device includes:

an input circuit connected to the bus line for holding a first bus line signal on the bus line in response to a supply of the first logical output signal from the first semiconductor device; and

a second output circuit connected to the input circuit for supplying the bus line with the held first bus line signal following to a supply of the second logical output signal from the first semiconductor device, wherein the comparison circuit receives a second bus line signal from the second output circuit and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

19. (Previously Presented) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and one of the plurality of bus lines is a selected bus line, and the first output circuit corresponding to the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to non-selected bus lines supply the non-selected bus lines with signals each having a second logical value.

20. (Previously Presented) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line is adjacent to another bus line, and the first output circuit corresponding to the at least

one bus line supplies the at least one bus line with the first logical output signal having a first logical value, and the first output circuit corresponding to the another bus line supplies the another bus line with a signal having a second logical value.

21. (Previously Presented) The electronic device of claim 18, wherein the first output circuit is one of a first group of first output circuits corresponding to a first group of the bus lines adjacent to a second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group of the first output circuits supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group of the first output circuits supplies the second group of the bus lines with signals each having a second logical value.

22. (Original) The electronic device of claim 18, wherein the first output circuit is used in a test mode and a normal operation mode of the first semiconductor device.

23. (Original) The electronic device of claim 18, wherein the input circuit and the second output circuit are used in a test mode and a normal operation mode of the second semiconductor device.

24. (Previously Presented) A first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with a plurality of bus lines, the first semiconductor device comprising:

an output circuit connected to one of the plurality of bus lines that supplies the bus line with a first logical output signal, wherein the second semiconductor device receives a first bus line signal on the bus line in response to a supply of the first logical

output signal from the output circuit and supplies the bus line with a second logical output signal being an inverted signal of the first bus line signal; and

a comparison circuit connected to the bus line, that receives a second bus line signal on the bus line in response to an output of the second logical output signal from the second semiconductor device and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

25. (Previously Presented) A first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with a plurality of bus lines, the first semiconductor device comprising:

an output circuit connected to one of the plurality of bus lines that supplies the bus line with a first logical output signal and, thereafter, supplies a second logical output signal being an inverted signal of the first logical output signal, wherein the second semiconductor device receives a first bus line signal on the bus line in response to a supply of the first logical output signal from the output circuit, and wherein the second semiconductor device holds a first bus line signal on the bus line in response to a supply of the first logical output signal from the first semiconductor device and supplies the bus line with the held first bus line signal following a supply of the second logical output signal from the first semiconductor device; and

a comparison circuit connected to the bus line, that receives a second bus line signal from the second semiconductor device and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the

connection between the first semiconductor device and the second semiconductor device.

26. (Previously Presented) The electronic device of claim 11, wherein:

the input circuit comprises a latch circuit that receives a logical signal supplied from the second semiconductor device via one of the bus lines, and

the second output circuit comprises a logical circuit connected to the latch circuit that inverts the latched logical signal to generate an inverted logical signal.

27. (Previously Presented) The electronic device of claim 26, further comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

28. (Previously Presented) An electronic device of claim 18, wherein:

the input circuit comprises a latch circuit, and

the second output circuit comprises a logical circuit connected to the latch circuit.

29. (Previously Presented) The electronic device of claim 28, further comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

Claims 30-48 (Canceled).